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DESIGN HIGH SPEED COMPLEX VEDIC MULTIPLIER USING BRENT KUNG ADDER TECHNIQUE

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ABSTRACT

The main objective of this research paper is to design architecture for complex Vedic multiplier by rectifying the problems in the existing method and to improve the speed by using the Brent Kung adder with the help of hybrid square technique. The Vedic multiplier algorithm is normally used for higher bit length applications and ordinary multiplier is good for lower order bits. These two methods are combined to produce the high speed multiplier for higher bit length applications. The problem of existing architecture is reduced by removing bits from the remainders. The proposed algorithm is implementation Xilinx software with Vertex-7 device family

KEYWORDS: Vedic Multiplier, Complex Multiplier, Hybrid BK Adder, Xilinx Software.

1. INTRODUCTION

Arithmetic is the most established and most rudimentary branch of Mathematics. The name Arithmetic is gotten from the Greek word "arithmos". Number-crunching is utilized by nearly everybody, for errands extending from straightforward everyday work. Subsequently, the requirement for a speedier and productive Arithmetic unit in PCs is the fascinating subject over decades. The four fundamental activities in basic number juggling are expansion, subtraction, duplication and division. Duplication is the essential scientific task of scaling one number by another. Duplication is utilized in the present designing field covering numerous Digital Signal Processing (DSP) applications, for example, convolution, Fast Fourier Transform (FFT), sifting and in Arithmetic Logic units of a chip, microcontroller and the greater part of the Embedded controllers. The interest for fast handling has been expanding because of extending PC and flag preparing applications. Higher throughput math tasks are basic to accomplish the coveted execution in some continuous flag and picture preparing applications. One of the key number juggling activities in such applications is increase and the improvement of speedier multiplier circuit has been a subject of enthusiasm over decades. Decreasing the time deferral and power utilization are extremely basic necessities for some applications.

Parallel augmentation is utilized to meet out the present necessity. Two kinds of parallel augmentations are exhibit duplication and tree increase. The essential multiplier is a straightforward cluster multiplier and it is outlined in view of move and – include task. One of the cases for exhibit duplication is the Braun multiplier and is intended for unsigned paired numbers. For tree structure Wallace multiplier is planned and it is likewise for an unsigned paired numbers. In the cluster increase, for marked numbers Baugh – Wooley, Booth Multiplier and Modified Booth Algorithm (MBA) are utilized. Dadda is another sort of multiplier in view of tree structure and is utilized for the augmentation of the marked numbers. These regular paired multipliers for unsigned numbers are considered for correlation. Vedic arithmetic is the arrangement of science followed in antiquated India and for the most part manages Vedic numerical formulae and their applications to different branches of math. The word 'Vedic' is gotten from the word 'Veda' which implies the storage facility of all learning.

Vedic arithmetic was reproduced from the antiquated Indian sacred texts (Vedas) by Sri Bharati Krishna Tirthaji (1884-1960), after his eight long stretches of research on Vedas. As indicated by his examination, Vedic arithmetic is mostly in view of sixteen standards or word-formulae and thirteen sub-end products which are

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named as Sutras. This is an extremely fascinating field and displays some compelling calculations which can be connected to different branches of Engineering, for example, computing and Digital Signal Processing. Vedic science lessens the multifaceted nature in estimations that exist in regular arithmetic. For the most part there are sixteen sutras accessible in Vedic arithmetic.

Among them just two sutras are material for augmentation activity. They are UrdhavaTriyakbhyam sutra (truly implies vertically and transversely) and Nikhilam Sutra (truly implies All from 9 and last from 10). Urdhava-Triyakbhyam is a non-specific technique for increase. The rationale behind UrdhavaTriyakbhyam sutra is particularly like the normal exhibit multiplier. Here the paired usage of this calculation is determined in view of a similar rationale utilized for decimal numbers. The paired usage of Nikhilam Sutra isn't yet fruitful.

This is a unique case in duplication. Another calculation used to streamline the increase procedure is Karatsuba calculation. This Karatsuba calculation utilizes a separation and-overcome approach where it separates the contributions to Most Significant half and Least Significant half and this procedure proceed until the point when the operands are of 8-bits wide. Karatsuba calculation is most appropriate for operands of higher piece length. In any case, at bring down piece lengths, it isn't as proficient as it is at higher piece lengths. This strategy was found by Anatoli Karatsuba in 1962. It diminishes the quantity of multipliers required, by supplanting the augmentation tasks by expansion activities. Expansion tasks are speedier than augmentations and subsequently the speed of the multiplier is expanded. As the measure of bits increment, the productivity of the multiplier will likewise increment.

In this exploration paper, a novel engineering of complex multiplier is planned utilizing half breed square kogge stone adder.

2. TYPES OF MULTIPLIER

Multipliers assume an essential part in the present advanced flag handling and different applications. Basic plan focuses of multiplier incorporate fast, low power utilization, consistency of design and thus less zone or even blend of them in one multiplier are required in this way making them appropriate for different VLSI usage.

Most duplication systems can be named Array multipliers and Tree multipliers. A point by point exchange on the distinctive sorts of multipliers is done in the accompanying segments.

(i) Array Multipliers

Exhibit multipliers can be actualized by straightforwardly mapping the manual duplication into equipment. The fractional items are collected by a variety of snake circuits. A n x n cluster multiplier requires (n-1) adders and n2 AND doors.

(ii) Carry Save Array Multiplier

The convey spare exhibit multiplier utilizes a variety of convey spare adders for the collection of incomplete item. It utilizes a convey proliferate viper for the age of the last item. This decreases the basic way deferral of the multiplier since the convey spare adders pass the convey to the following level of adders instead of the contiguous ones.

(iii) Wallace Tree Multiplier

C. S. Wallace (1964) propounded a quick strategy to perform augmentation. A Wallace tree multiplier offers speedier execution for extensive operands. Not at all like a cluster multiplier is the incomplete item network for a tree multiplier revamped in a tree-like configuration, diminishing both the basic way and the quantity of snake cells required.

(iv) Dadda Multiplier

Dadda multiplier is an equipment multiplier planned like Wallace multiplier. Dissimilar to Wallace multipliers that perform diminishments however much as could be expected on each layer, Dadda multipliers do as couple of decreases as could reasonably be expected. Because of this, Dadda multipliers have more affordable diminishment stage, however the numbers might be a couple of bit longer, along these lines requiring

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marginally greater adders. This infers less sections are packed in the underlying phases of the segment pressure tree, and more segments in the later levels of the multiplier.

(v) Booth Wallace Tree Multipliers

The utilization of Booth's calculation, in duplication shows a productive arrangement that suits the requests of fast multipliers, which likewise should be proficient as far as equipment plan/zone many-sided quality.

In this multiplier, the fractional items are produced utilizing the Booth technique, while their summation is finished utilizing Wallace tree structure. This packs the expansion procedure. The viper is utilized in snake gatherer setup, where the duplication result is added each opportunity to the fractional item enlist.

Table 1: Comparison of Multiplier

Types of Multiplier	Delay/ Increase in bit size	Structure/ Complexity	Area	Speed
Array	Linear	Regular/ Low	High	Low
Wallace	Logarithmic	Irregular/ High	High	High
Dadda Tree	Logarithmic	Irregular/ High	High	High
Booth	Non-linear	Regular/ Medium	Low	Mediu m

3. VEDIC MULTIPLIER

Vedic multiplier and hybrid square KoggeStone adder can contrast and traditional technique which is processed by Vedic multiplier, full snake and half viper. Proposed system gives less way delay and less territory. Info succession of Conventional strategy is substantially more than to proposed technique; anyway proposed strategy has less spread postponement. Zone and proliferation deferral can be lessened by the guide of half and half square Kogge Stone snake. This snake will be outlined like as swell convey viper.

Rationale Diagram of Vedic Multiplier utilizing Kogge Stone Adder is appeared in figure 1. In the long run, all the planning levels of advanced framework or IC's Packages rely upon number of entryways in a solitary chip that is likewise rung base approach. Changed KS viper can be diminished with respect to the zone or number of entryways. In the event that we expel the primary XOR door from altered KS snake nothing will be changed for result yet territory and engendering postponement will be decreased.

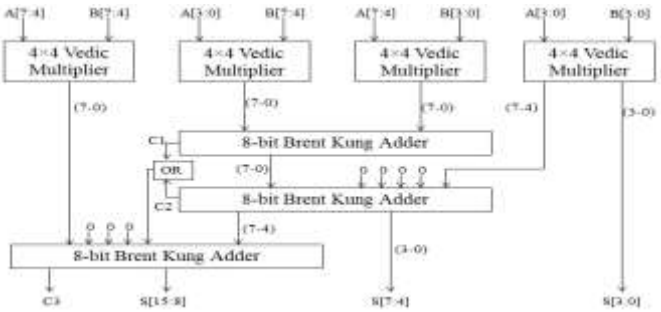

Figure 1: 8-bit Vedic Multiplier using Hybrid Brent Kung Adder

(i) Hybrid Brent Kung Adder

The total working of KSA can be effectively understood by investigating it as far as three particular parts:

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(a) Preprocessing: - This progression includes calculation of create and spread signs comparing too each combine of bits in An and B. These signs are given by the rationale conditions beneath:

$$P_i = A_i \, xor \, B_i \quad (1)$$

$$G_i = A_i \, and \, B_i \quad (2)$$

(b) Carry look ahead network: -This square separates KSA from different adders and is the primary power behind its superior. This progression includes calculation of conveys comparing to each piece.

$$C_i = G_i \, or \, (P_i \, and \, C_{i-1}) \quad (3)$$

(c) Post processing: - This is the last advance and is normal to all adders of this family (convey look forward). It includes calculation of total bits. Total bits are figured by the rationale given underneath:

$$S_i = P_i \, xor \, C_{i-1} \quad (4)$$

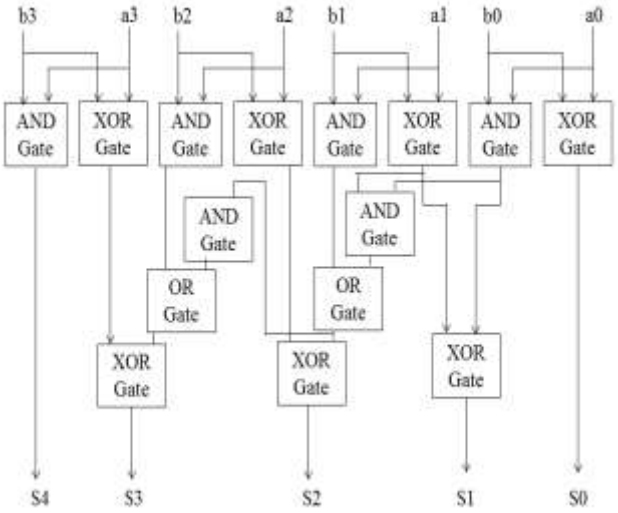

Figure 2: 4-bit BrentKung Adder

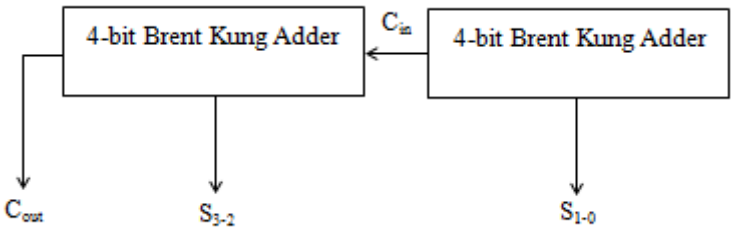

Figure 3: 8-bit Hybrid Brent Kung Adder

4. COMPLEX MULTIPLIER

Suppose two numbers are complex then

$$A = A_r + jA_i$$

$$B = B_r + jB_i$$

The product of A and B then

$$P = A \times B$$

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$$P = A_r \times B_r - A_i \times B_i + j(A_r \times B_i + A_i \times B_r)$$
$$P_r = A_r \times B_r - A_i \times B_i$$
$$P_i = A_r \times B_i + A_i \times B_r$$

Where $P_r$and P_i is represents the real and imaginary part of the output of the complex multiplier. A_r and $A_i$is represents the real and imaginary part of the first input of the complex multiplier. B_r and $B_i$is represents the real and imaginary part of the second input of the complex multiplier.

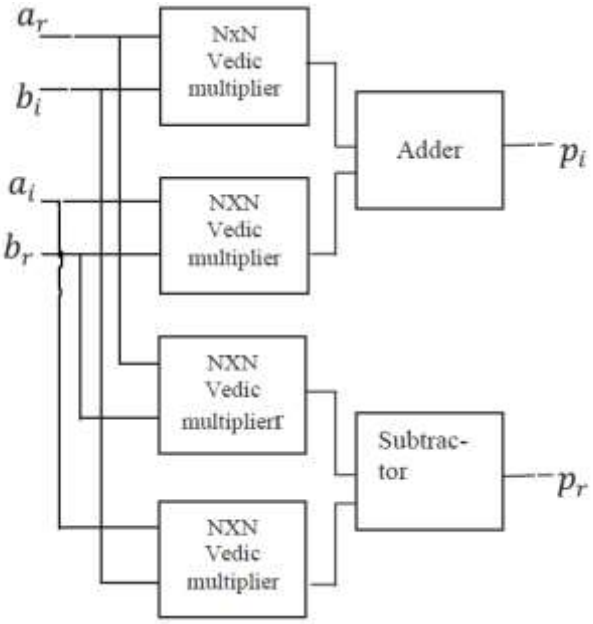

Figure 5: Block Diagram of Complex Multiplier for four Vedic Multiplier

Complex multiplier for four Vedic multipliers is shown in figure 5. In this block diagram reduce four Vedic multipliers to three Vedic multipliers is shown in below:

$$P_r = A_r \times B_r - A_i \times B_i = A_r(B_r + B_i) - B_i(A_r + A_i)$$
$$P_i = A_r \times B_i + A_i \times B_r = A_r(B_r + B_i) + B_r(A_i - A_r)$$

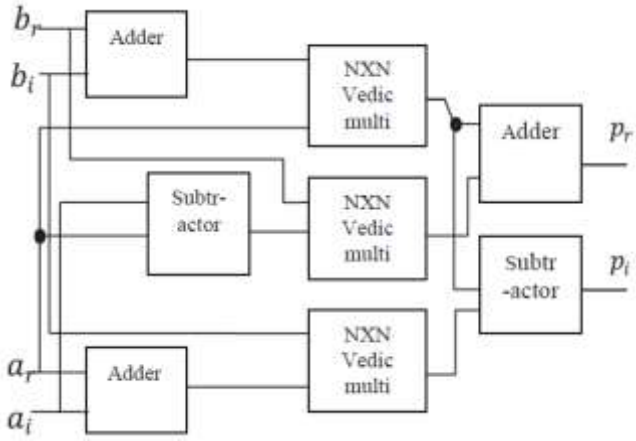

Figure 6: Block Diagram of Complex Multiplier for three Vedic Multiplier

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5. SIMULATION ANALYSIS

Reproduction of these trials should be possible by utilizing Xilinx 14.2 I VHDL instrument. In this paper we are concentrating on proliferation delay. Spread defer must be less for better execution of advanced circuit.

As shown in table II the number of slice, numbers of LUTs, delay are obtained for the Vedic multiplier using hybrid square BK adder and previous algorithm. From the analysis of the results, it is found that the Vedic multiplier using hybrid square BK adder gives a superior performance as compared with previous algorithm for Spartan-3 device family.

Table II: Comparison Result for 8-bit Vedic Multiplier

Design	Number of Slice	Number of LUTs	Delay
Vedic Multiplier using Full Adder [1]	111	198	-
Vedic Multiplier using Ripple Carry Adder	102	178	25.077 ns
Vedic Multiplier using Brent Kung Adder	93	158	17.380 ns

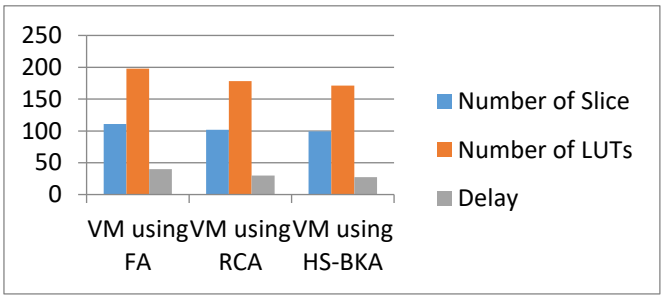

Figure 7: Bar graph of the 8-bit Vedic multiplier

Figure7 demonstrates the graphical outline of the execution of VM utilizing BKA calculation examined in this examination work in term of number of cut, number of LUTs and deferral. From the above graphical portrayal it can be construed that the VM utilizing BKA calculation gives the best execution as contrasted and past calculation.

As appeared in table III the quantity of LUTs, delays are gotten for the complex Vedic multiplier utilizing cross breed square BK adder and past calculation. From the investigation of the outcomes, it is discovered that the complex Vedic multiplier utilizing half and half square adder gives an unrivaled execution as contrasted and past calculation for Vertex-7 gadget family. The yield waveform of the 32-bit complex multiplier utilizing half and half square BK adder is appeared in figure 8 and figure 9 individually.

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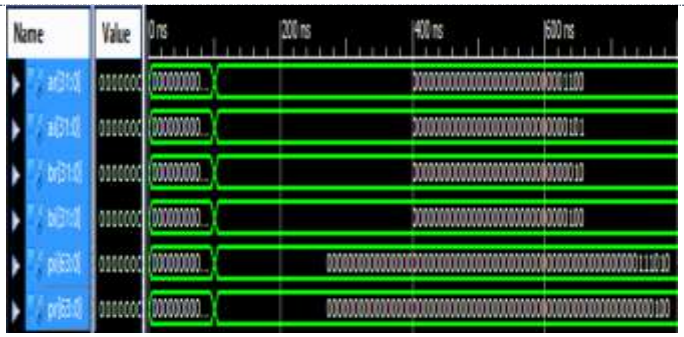

Figure 8: Output Binary Waveformof 32-bit Complex Multiplier using HS-BKA

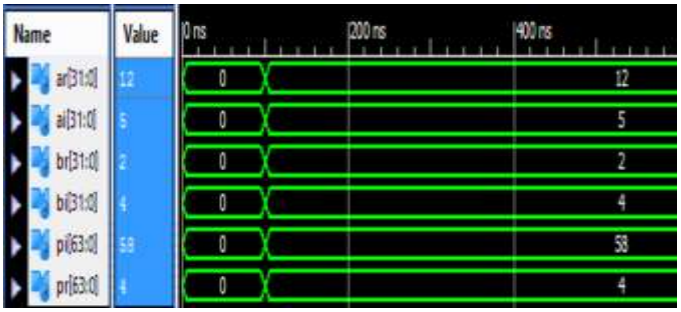

Figure 9: Output Decimal Waveformof 32-bit Complex Multiplier using HS-BKA

Table III: Comparison Result for 32-bit Complex Vedic Multiplier for four Vedic Multiplier

Design	Number of LUTs	Number of IOBs	Delay
Complex Vedic Multiplier [2]	10416	256	25.979 ns
Complex Vedic Multiplier using Ripple Carry Adder	10642	256	26.927 ns
Complex Vedic Multiplier using Hybrid Brent Kung Adder	10742	256	21.00 ns
Percentage (%)	3.03 decrease by base paper	0%	19.16% improve by base paper

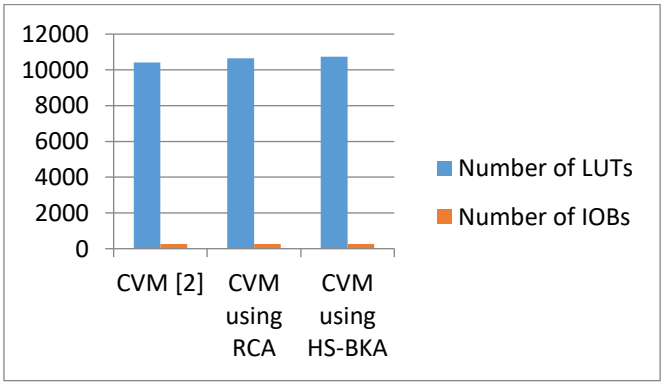

Figure 10: Bar graph of the 32-bit Complex Vedic multiplier

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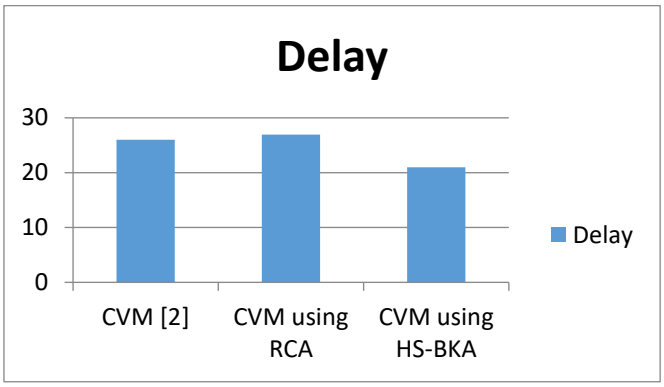

Figure 11: Bar graph of the 32-bit Complex Vedic multiplier

Figure10 and figure 11 shows the graphical illustration of the performance of CVM using BKA algorithm discussed in this research work in term of number of slice, number of LUTs and delay. From the above graphical representation it can be inferred that the CVM using BKA algorithm gives the best performance as compared with previous algorithm.

6. CONCLUSION

In this paper design of hybrid square Brent Kung adder, Vedic multiplier and complex Vedic multiplier is presented. From implementation results it is observed that the hybrid based Vedic Multiplier and complex Vedic multiplier consumes less delay compare to previous design.

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